

Fig.1

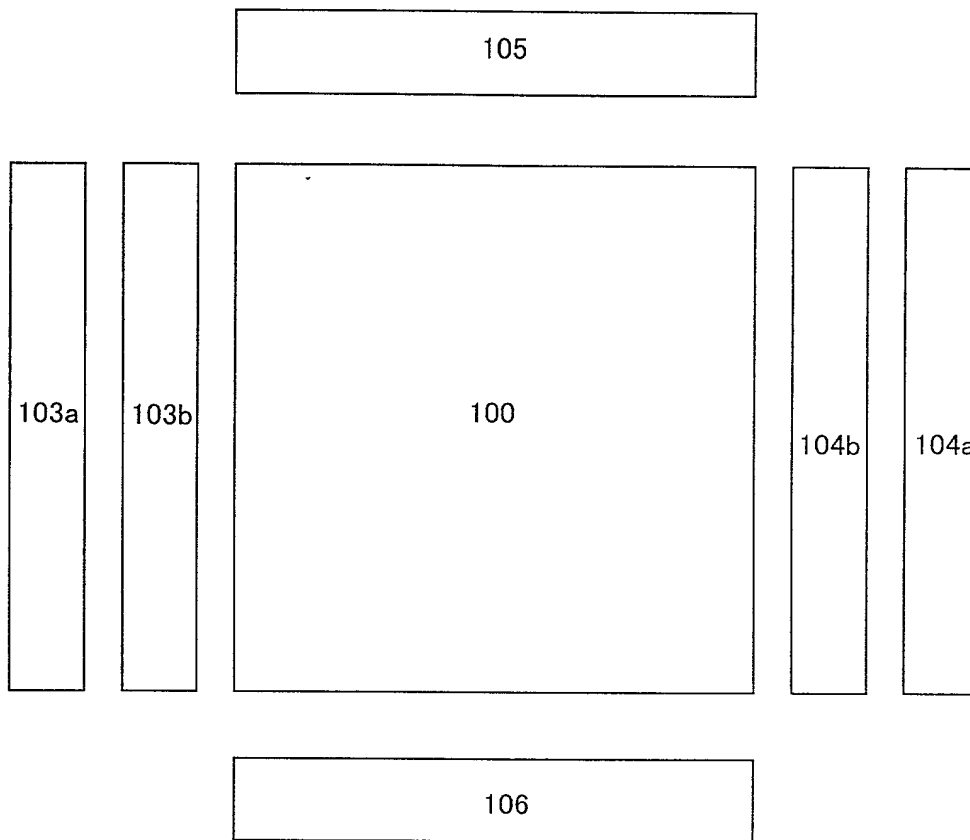




Fig.3

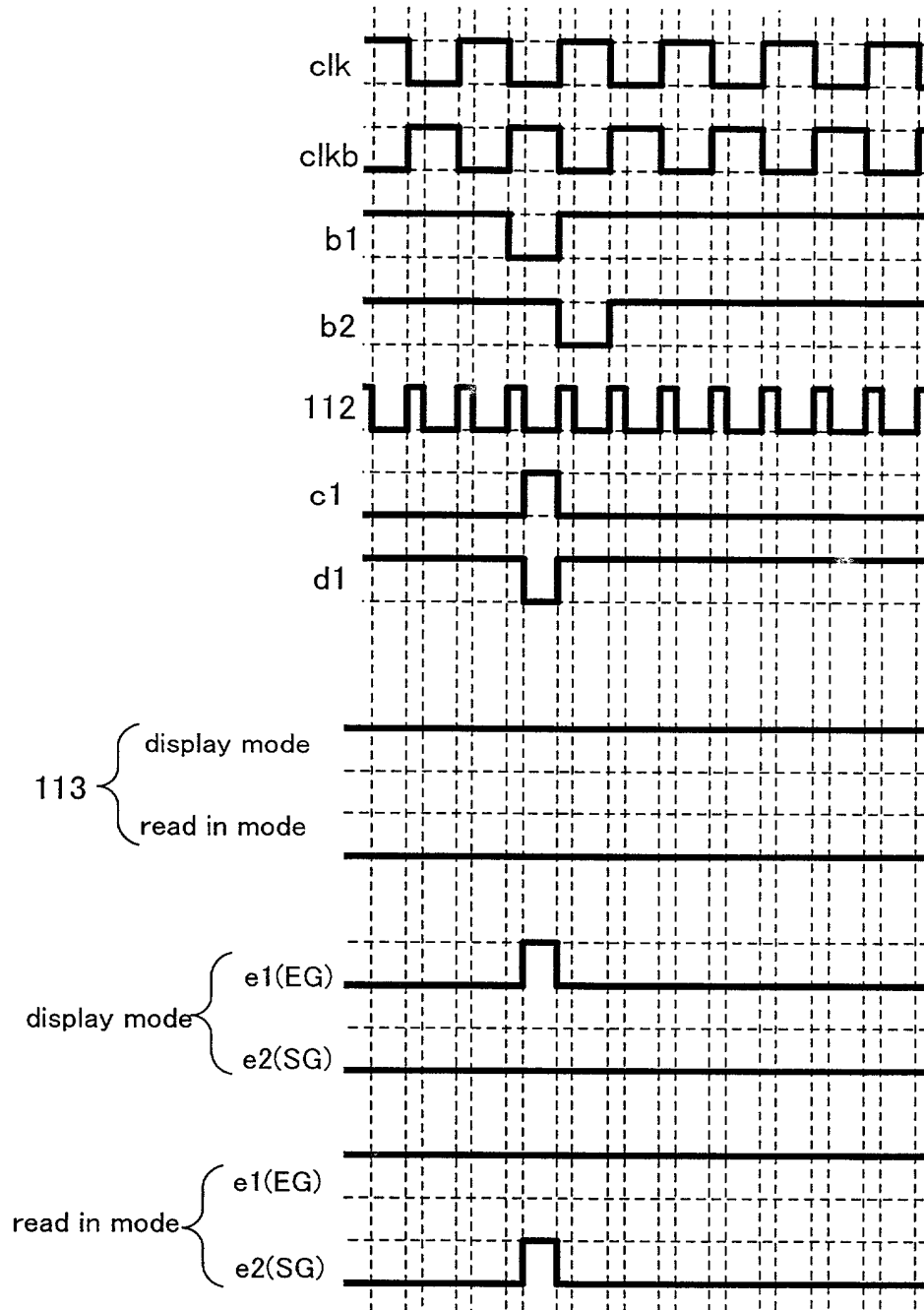


Fig.4A

		display mode	monochrome read in
light emitting element portion	source signal line driver circuit	pulse	on
	video signal	pulse	on
	EG	pulse	on
	ER	pulse	off
sensor portion	SS		pulse
	SG	off	pulse
	SR	off	pulse

Fig.4B

		display mode	color read in		
			R	G	B
light emitting element portion	source signal line driver circuit	pulse	on	on	on
	video signal (R)	pulse	on	off	off
	video signal (G)	pulse	off	on	off
	video signal (B)	pulse	off	off	on
	EG	pulse	on	on	on
	ER	pulse	off	off	off
sensor portion	SS		pulse	pulse	pulse
	SG	off	pulse	pulse	pulse
	SG	off	pulse	pulse	pulse

Fig.5

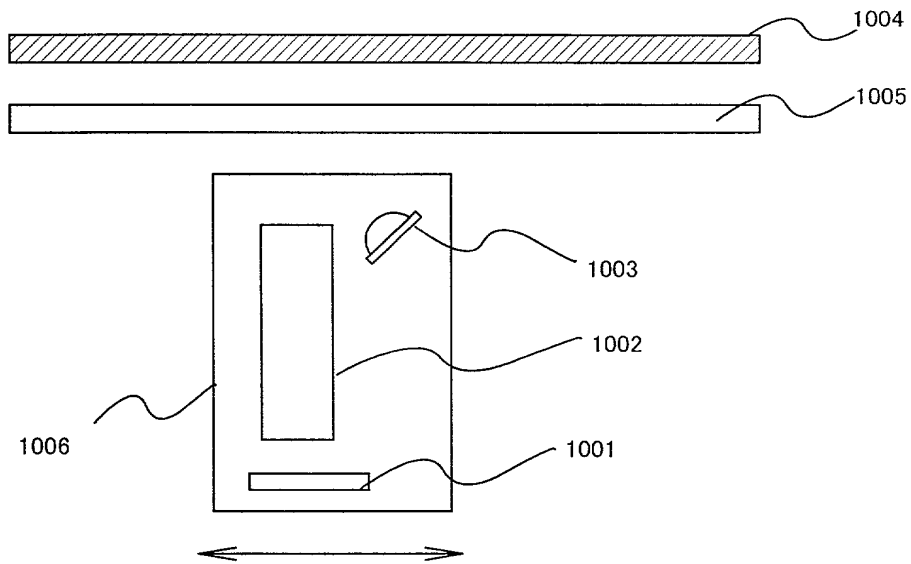


Fig.6

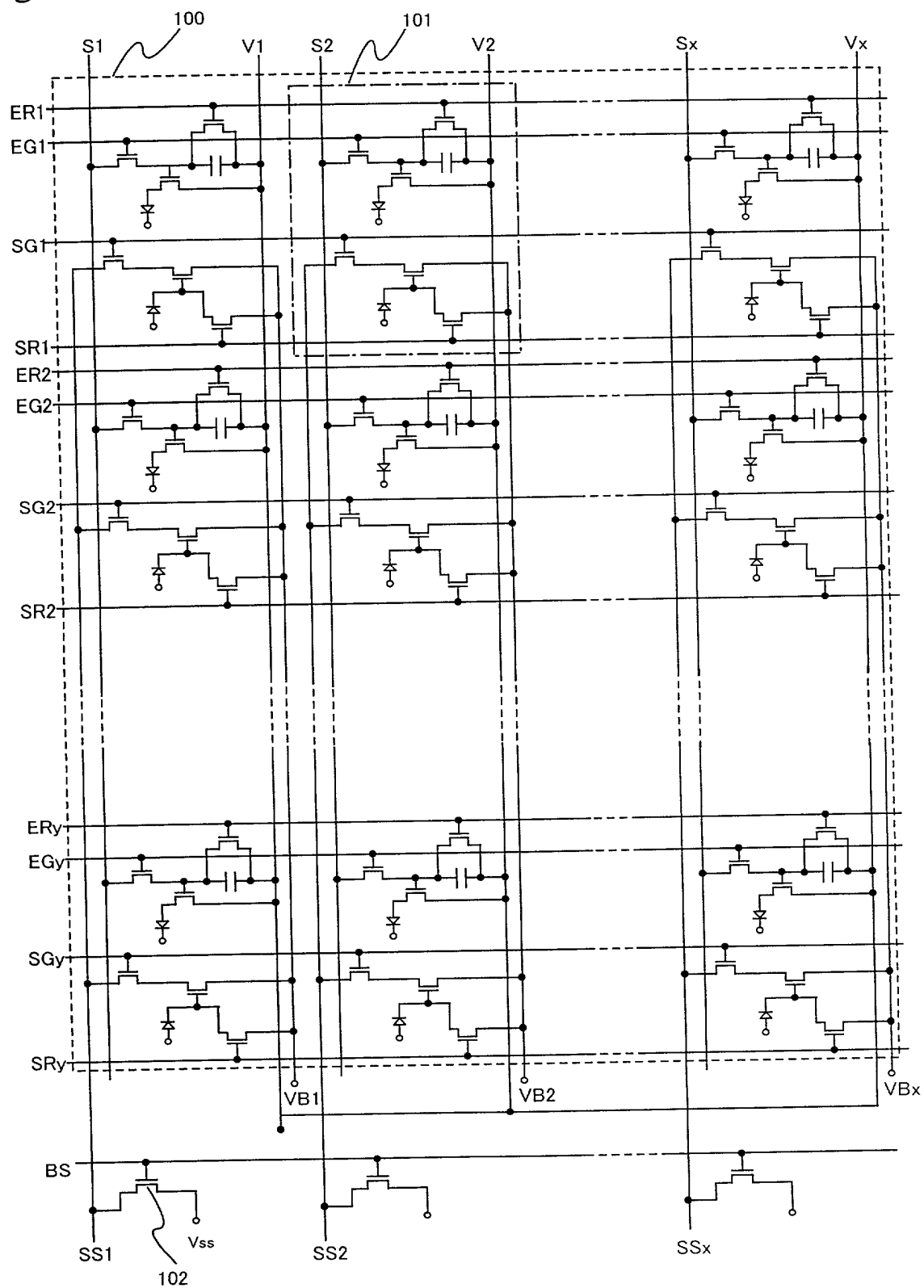


Fig.7

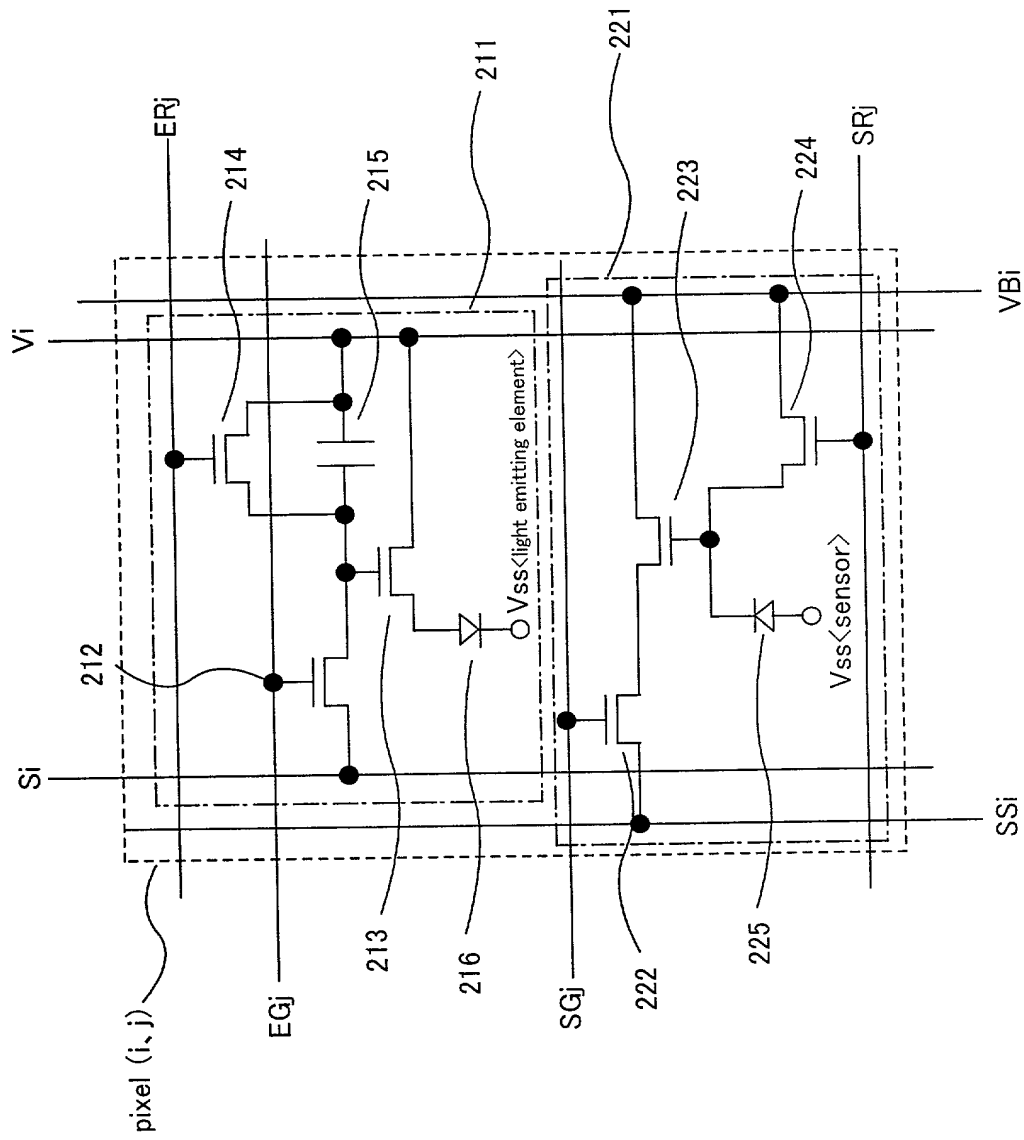


Fig.8

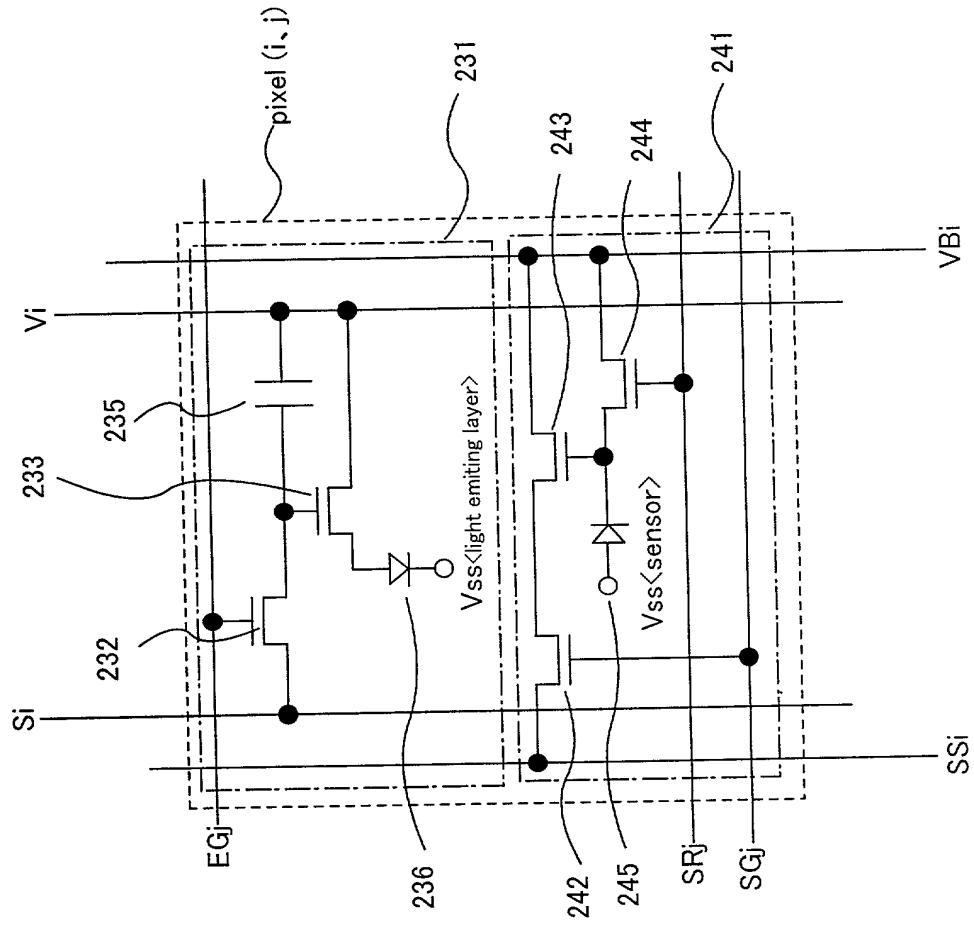






Fig.10

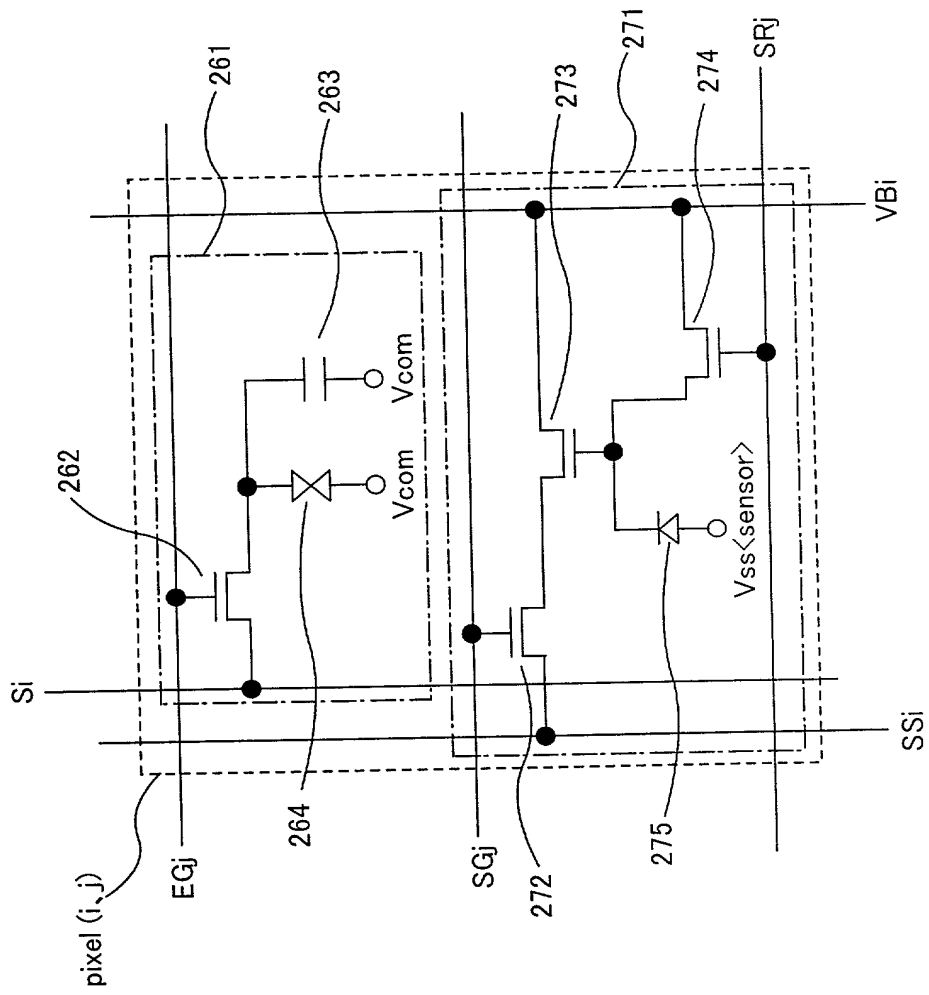


Fig.11

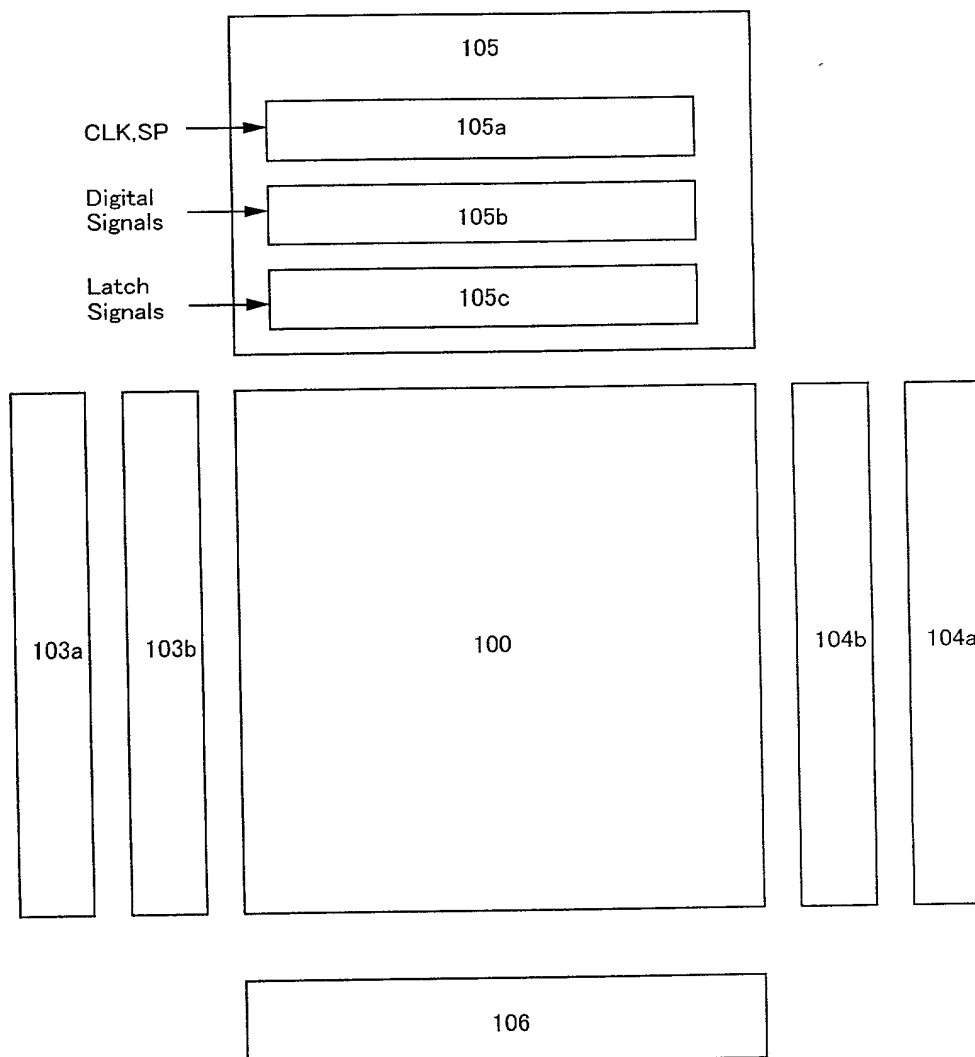


Fig.12

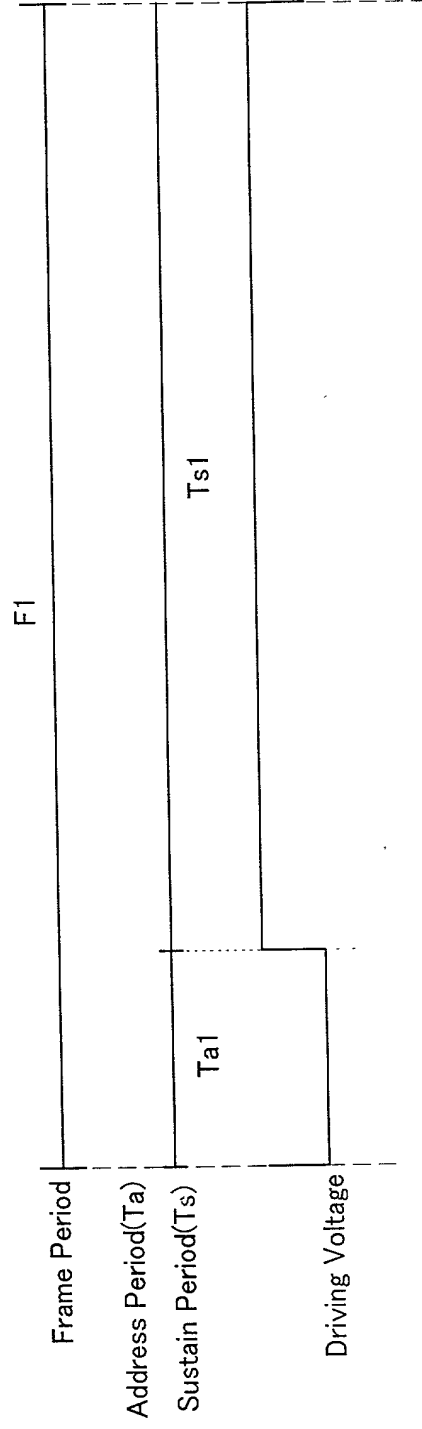


Fig.13

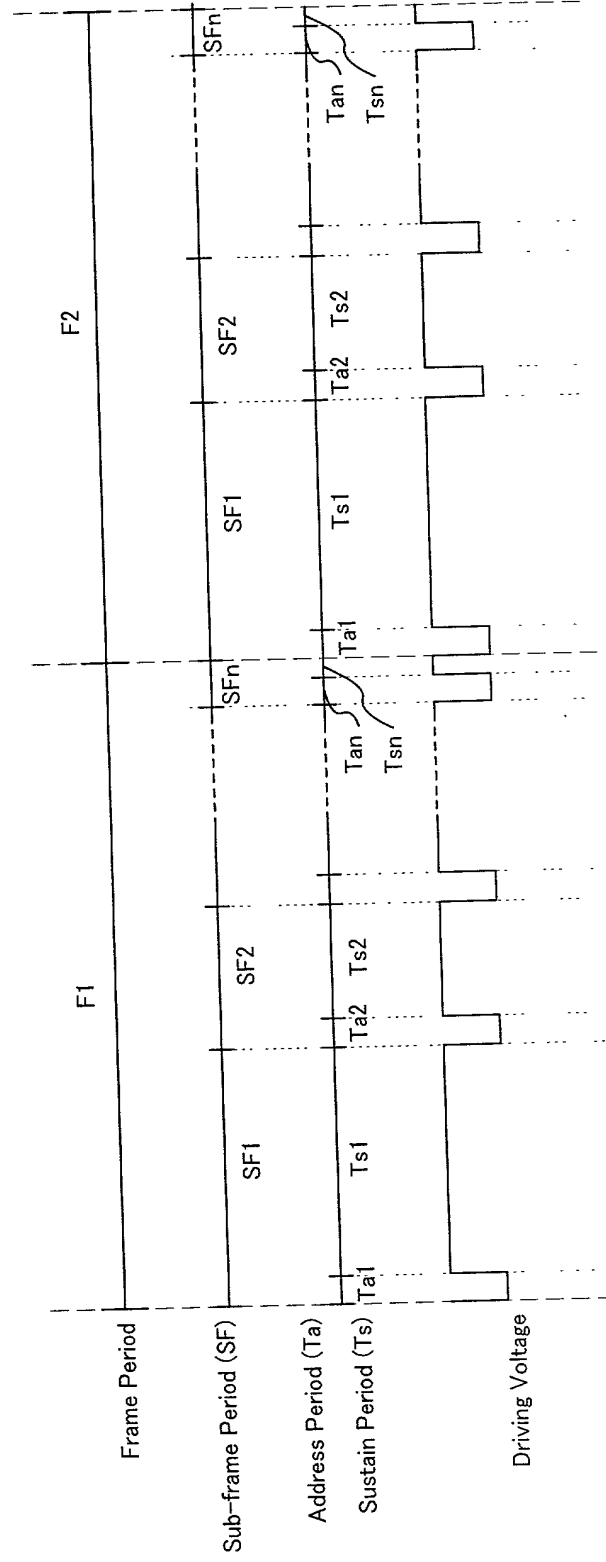


Fig.14

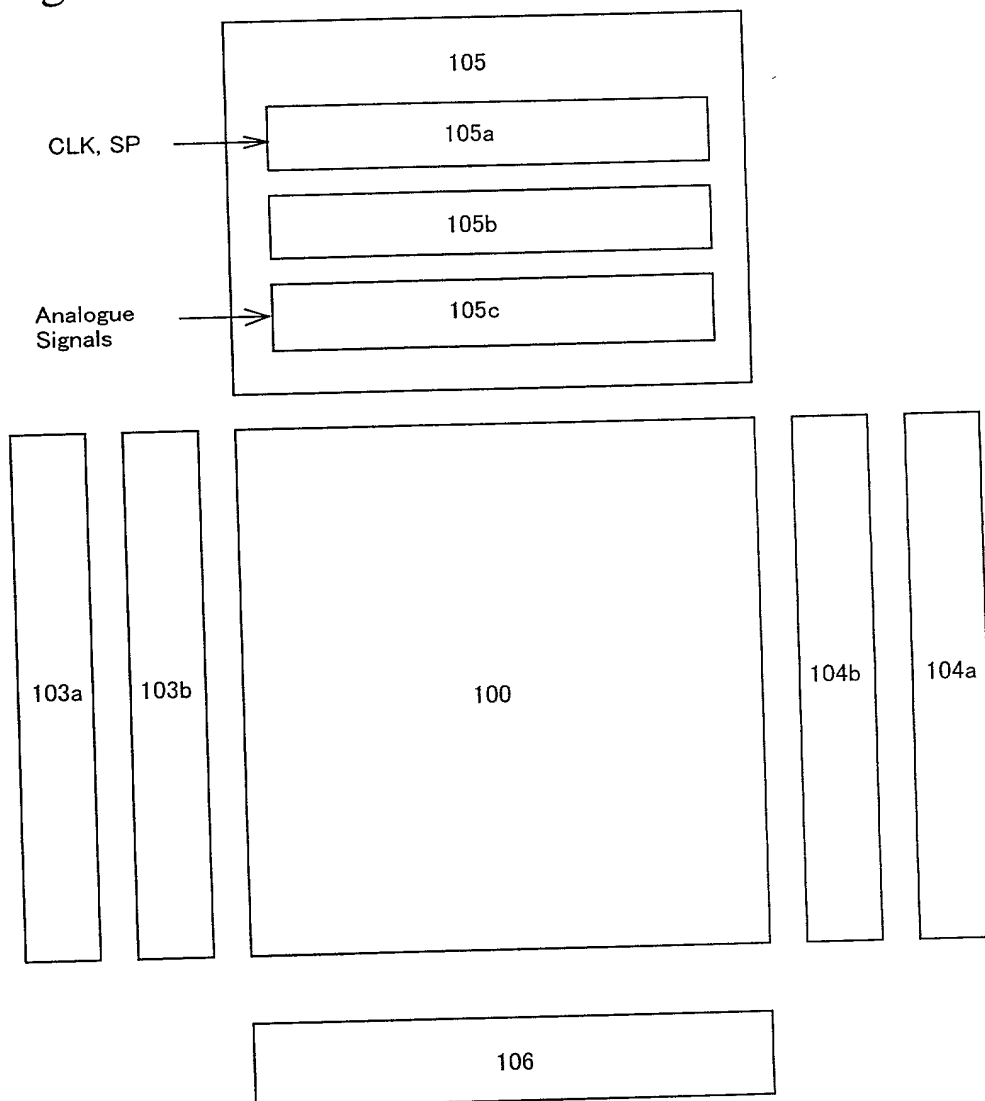


Fig.15

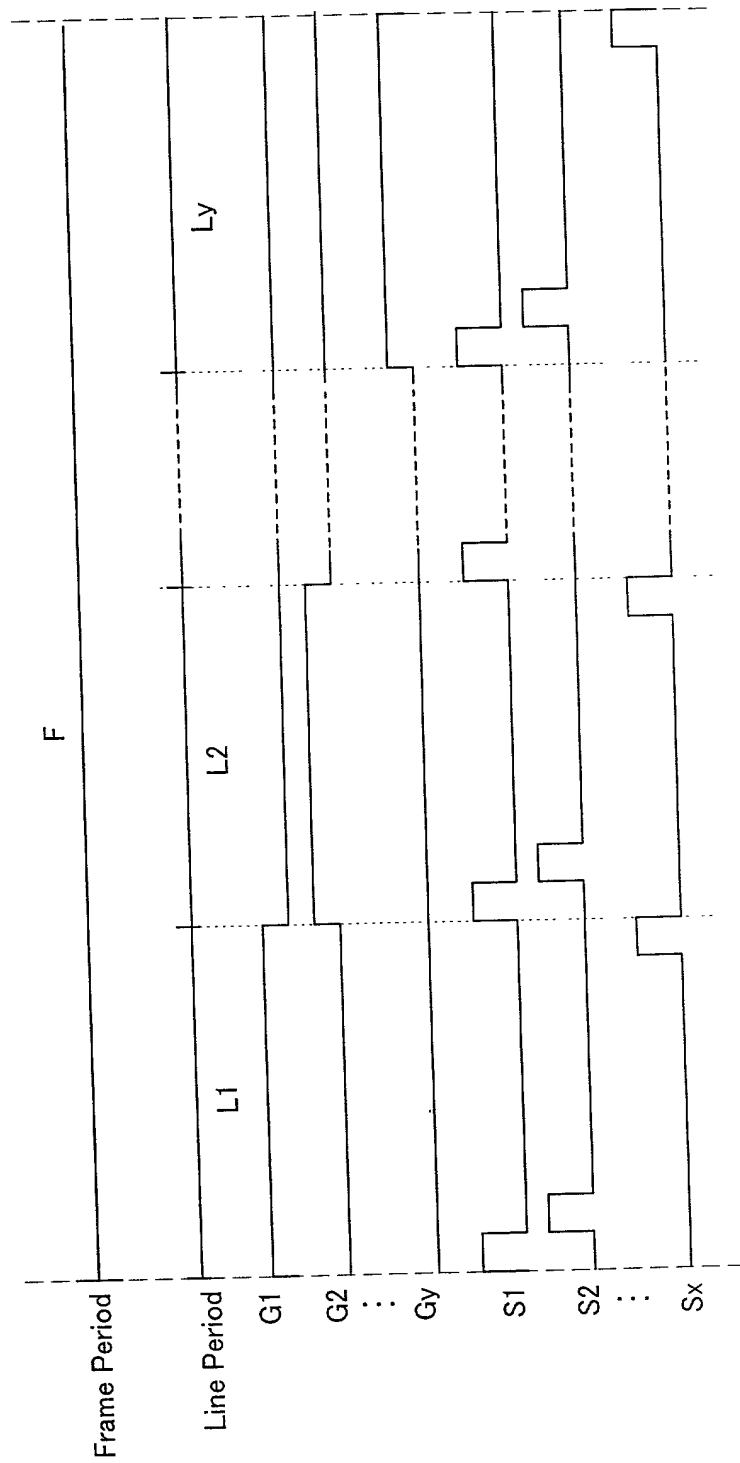


Fig.16

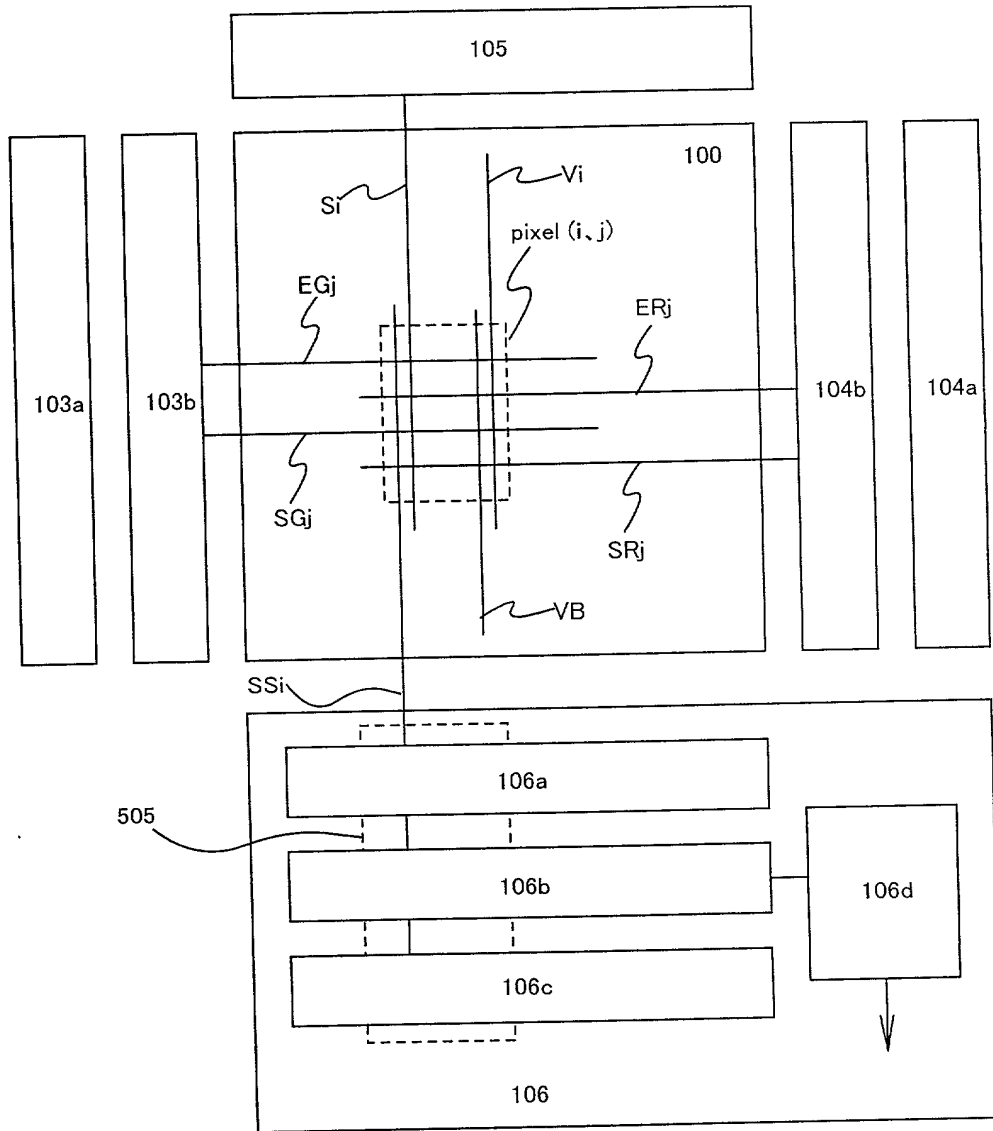




Fig.17

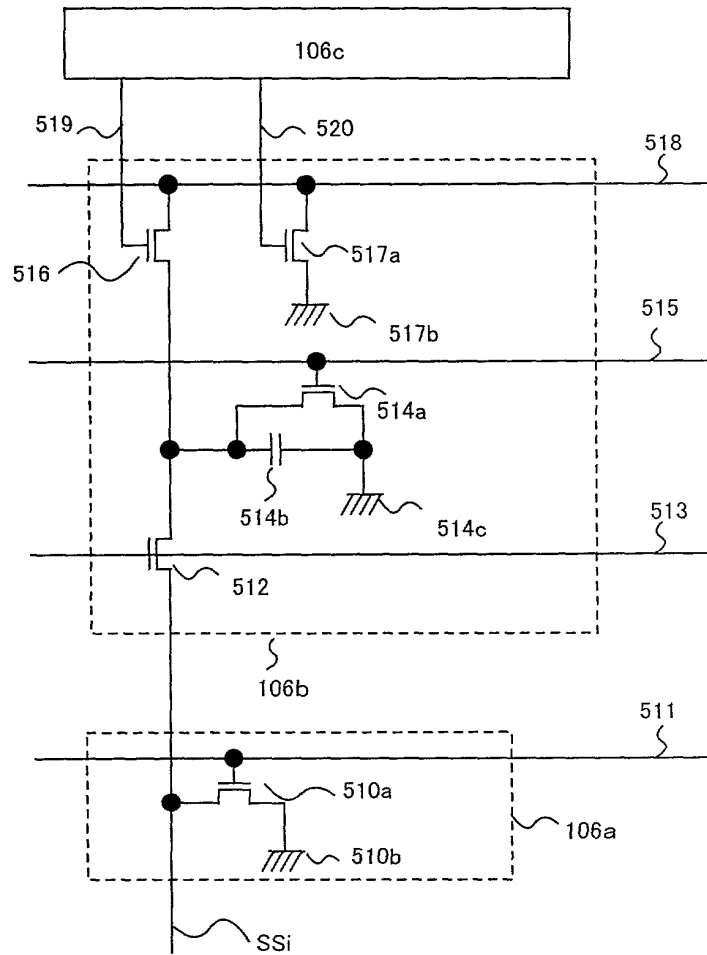


Fig.18

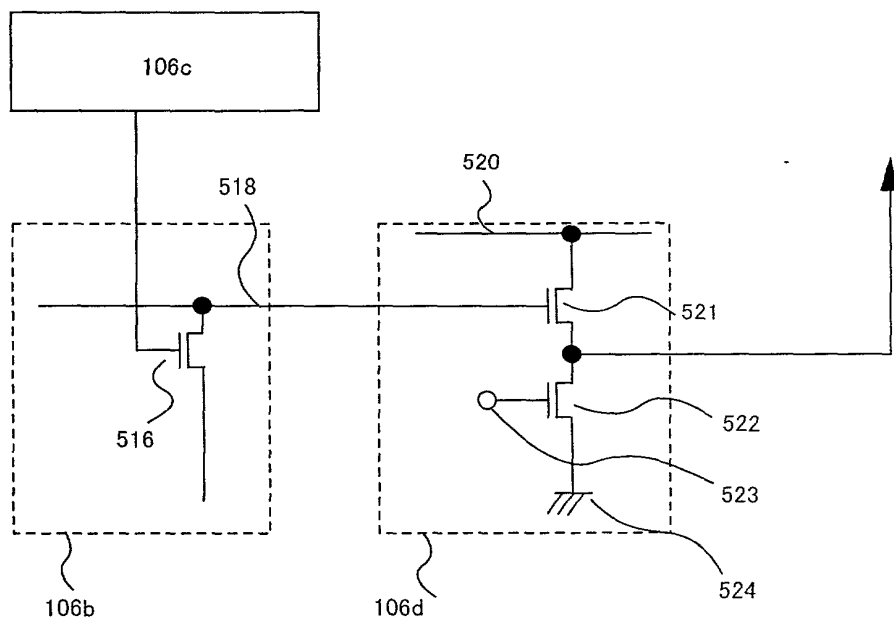


Fig.19

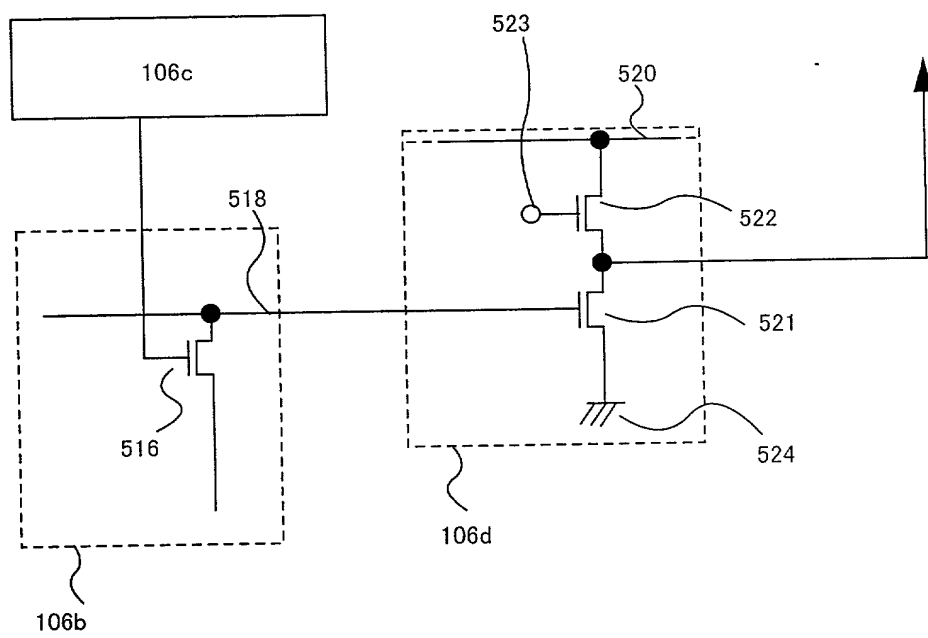
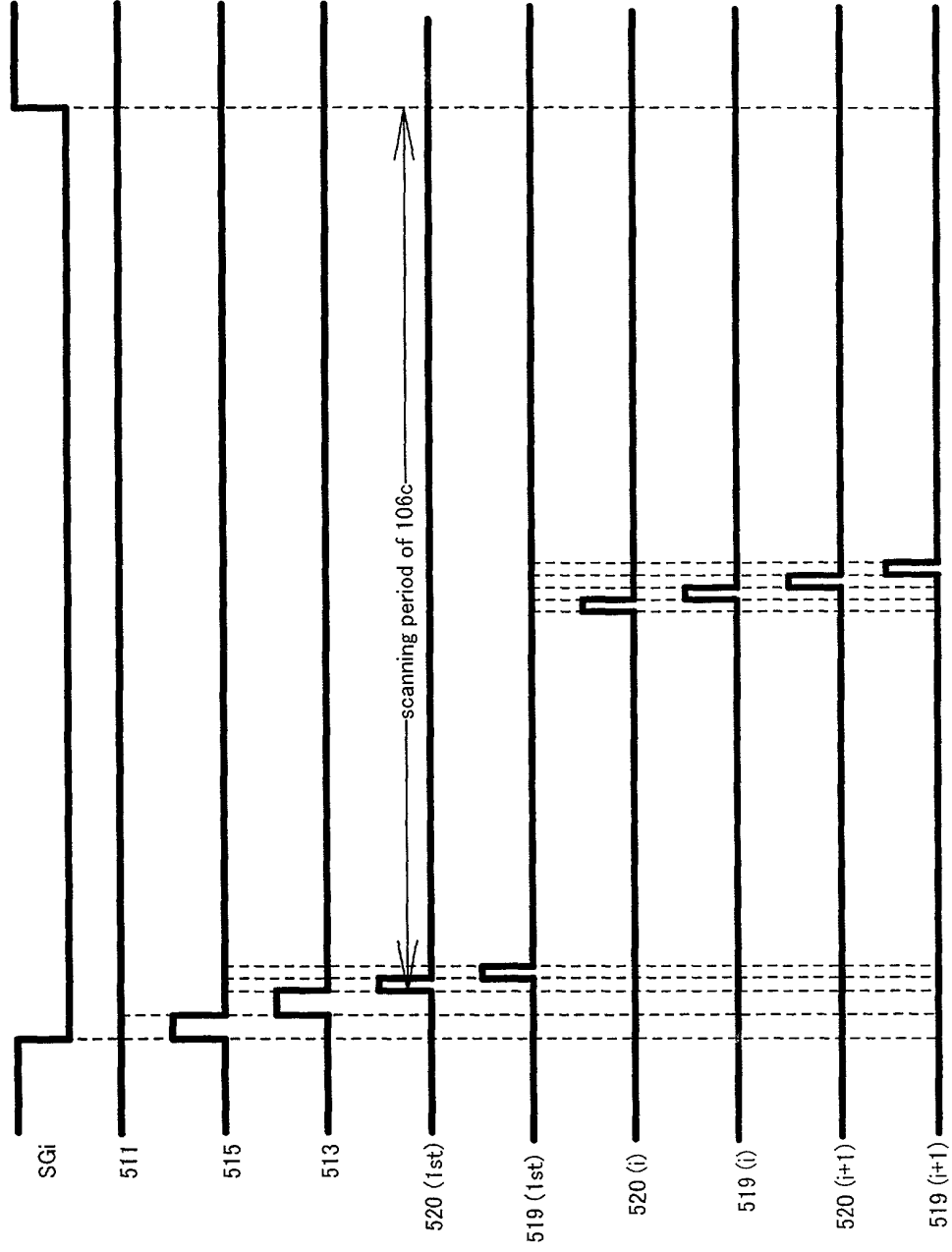


Fig.20





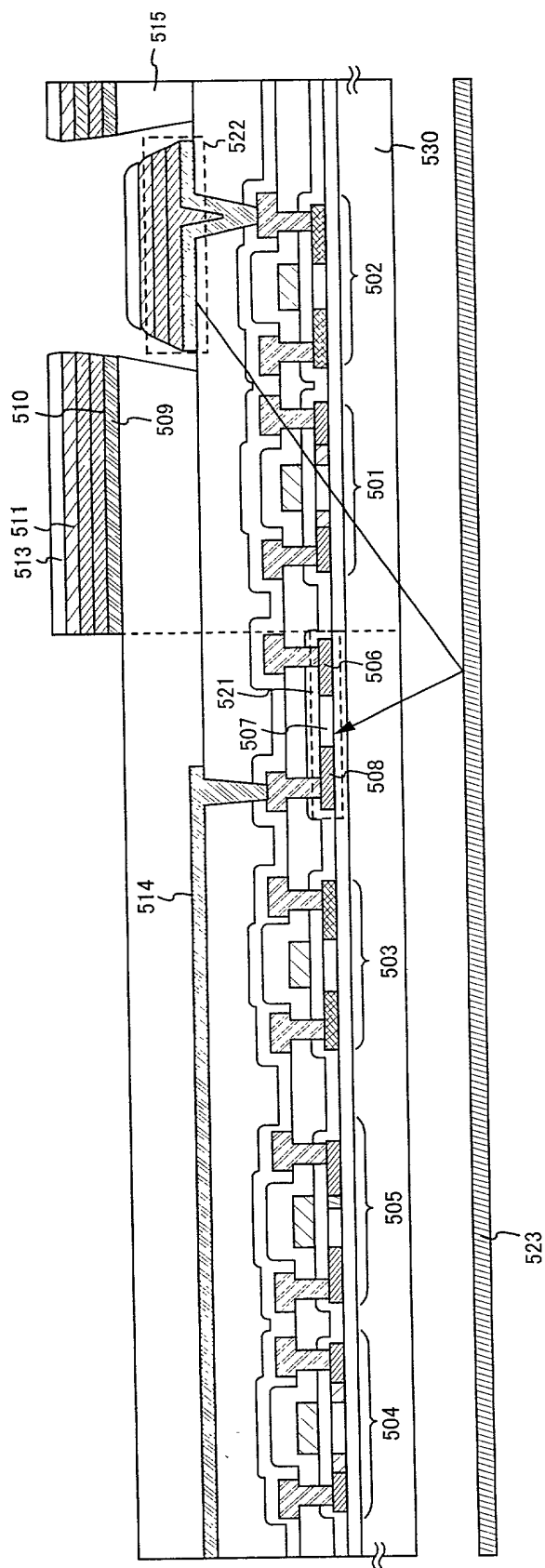


Fig.23

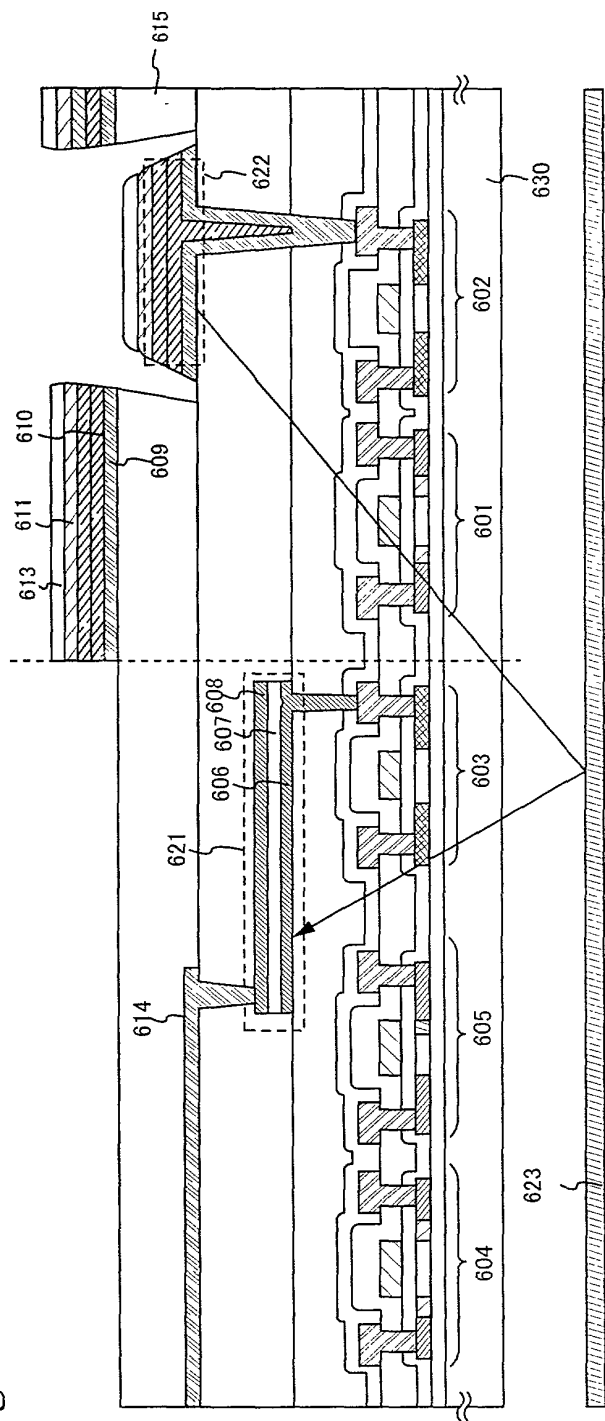


Fig.24

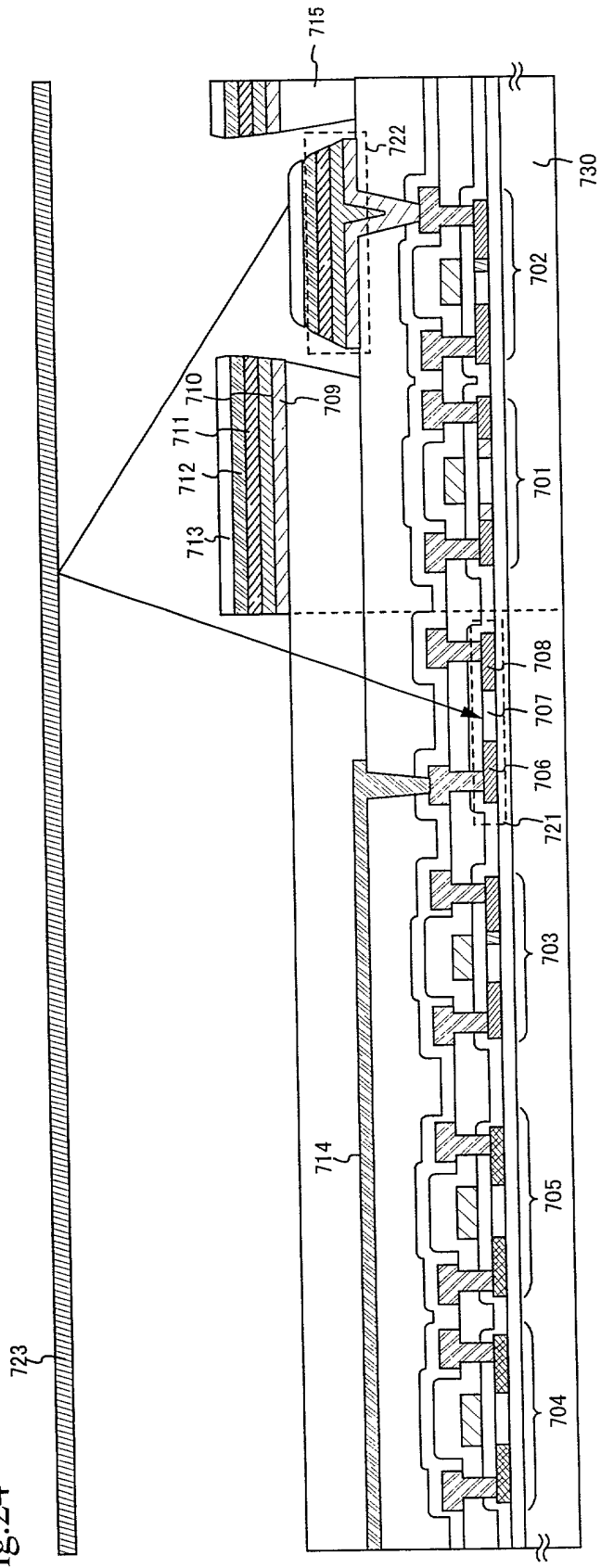




FIG. 25 is a cross-sectional view of a semiconductor device, showing a substrate 800 with a series of layers 801, 802, 803, 804, 805, 806, 807, 808, 809, 810, 811, 812, 813, 814, 840, and 823. The device includes a gate stack 801, a channel layer 802, a source/drain region 803, a contact layer 804, a passivation layer 805, a protective layer 806, a buffer layer 807, a seed layer 808, a sacrificial layer 809, a hard mask 810, a photoresist 811, a photoresist 812, a photoresist 813, a photoresist 814, a photoresist 840, and a photoresist 823.

Fig.25

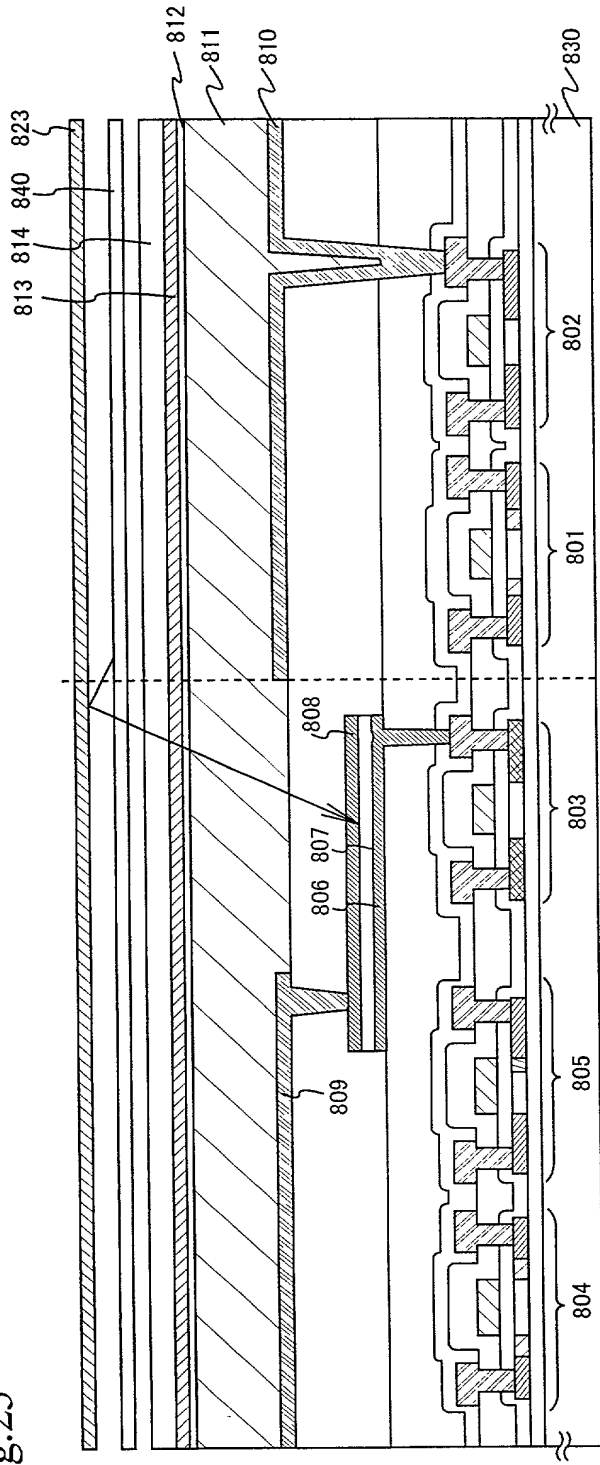


FIG. 26 is a cross-sectional view of a semiconductor device 900, showing a substrate 901, a gate stack 902, a source/drain region 903, a contact pad 904, and a passivation layer 905. The device includes a gate electrode 906, a gate insulating layer 907, a gate conductive layer 908, a source/drain conductive layer 909, a contact conductive layer 910, a contact insulating layer 911, and a passivation layer 912. The device is formed on a substrate 901, which is a semiconductor material. The gate stack 902 is formed on the substrate 901, and the source/drain region 903 is formed in the substrate 901. The contact pad 904 is formed on the source/drain region 903, and the passivation layer 905 is formed on the contact pad 904. The gate electrode 906 is formed on the gate stack 902, and the gate insulating layer 907 is formed on the gate electrode 906. The gate conductive layer 908 is formed on the gate insulating layer 907, and the source/drain conductive layer 909 is formed on the source/drain region 903. The contact conductive layer 910 is formed on the contact pad 904, and the contact insulating layer 911 is formed on the contact conductive layer 910. The passivation layer 912 is formed on the contact insulating layer 911.

Fig.26

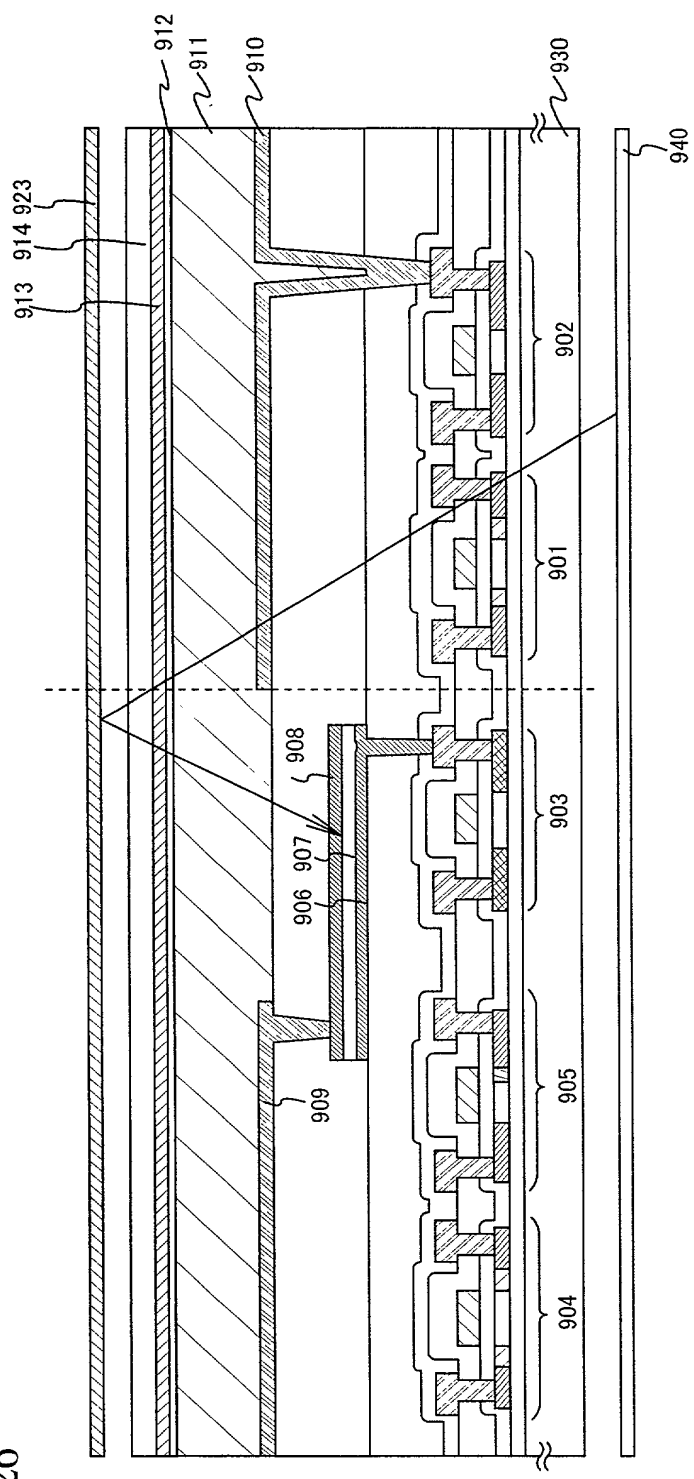


Fig.27A

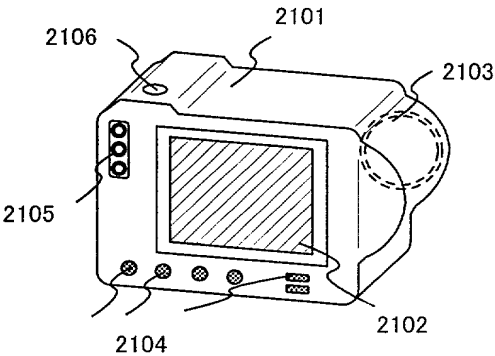


Fig.27B

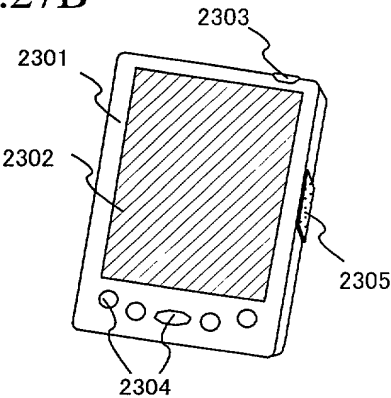


Fig.27C

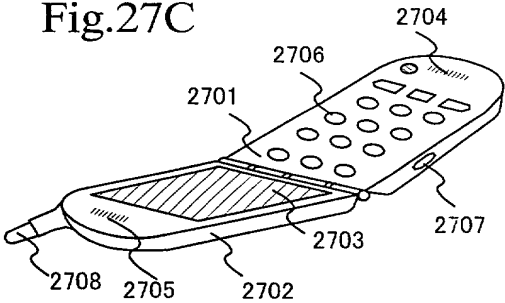


Fig.28A

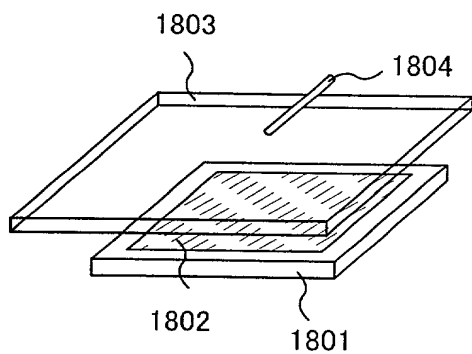


Fig.28B

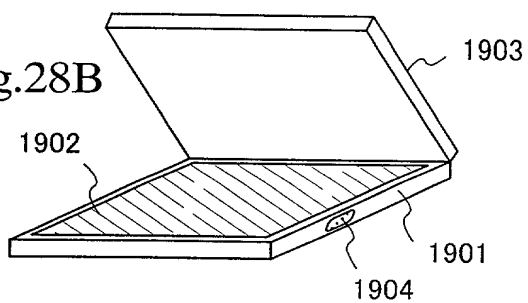


Fig.28C

